Surface Mount Fast Recovery Rectifier Diode

Features

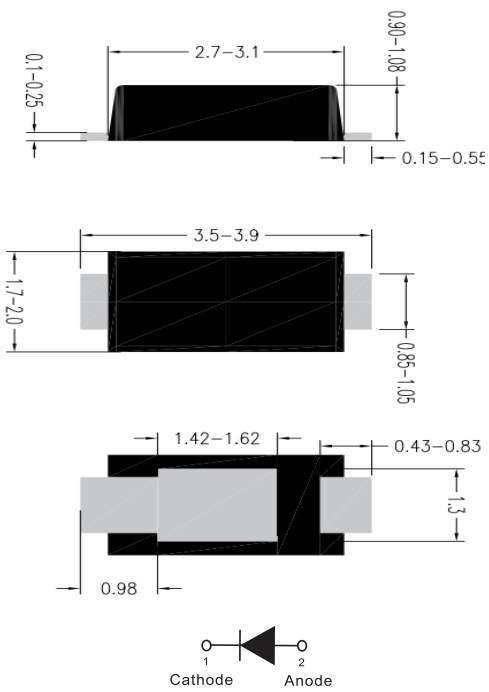
- Low profile package
- Ideal for automated placement
- Glass passivated chip junction
- Fast switching for fast recovery
- High forward surge capability
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260°C

Mechanical Data

- **Package**: SOD-123HE
  Molding compound meets UL 94 V-0 flammability rating, RoHS-compliant, halogen-free
- **Terminals**: Tin plated leads, solderable per J-STD-002 and JESD22-B102
- **Polarity:** Cathode line denotes the cathode end

SOD-123HE

Unit : inch(mm)



Maximum Ratings and Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	RS1A HE	RS1B HE	RS1D HE	RS1G HE	RS1J HE	RS1K HE	RS1M HE	Unit
Maximum repetitive peak reverse voltage	V_{RRM}	50	100	200	400	600	800	1000	V
Maximum RMS voltage	V_{RMS}	35	70	140	280	420	560	700	V
Maximum DC blocking voltage	V_{DC}	50	100	200	400	600	800	1000	V
Maximum average forward rectified current	$I_{F(AV)}$	1							A
Peak forward surge current, 8.3 ms single half sine-wave superimposed on rated load	I_{FSM}	30							A
Maximum instantaneous forward voltage (Note 1) @1A	V_F	1.3							V
Maximum reverse current @ rated V_R T_J=25°C T_J=125°C	I_R	5 50							μA
Maximum reverse recovery time (Note 2)	t_{rr}	150				250	500		ns
Typical junction capacitance (Note 3)	C_J	10							pF
Typical thermal resistance	$R_{\theta JC}$ $R_{\theta JA}$	45 90							°C/W
Operating junction temperature range	T_J	- 55 to +150							°C
Storage temperature range	T_{STG}	- 55 to +150							°C

Note:

1. Pulse test with PW=300μs, 1% duty cycle
2. Reverse Recovery Test Conditions: I_F=0.5A, I_R=1.0A, I_{RR}=0.25A
3. Measured at 1 MHz and Applied Reverse Voltage of 4.0V D.C.

Ratings and Characteristic Curves (T_A=25℃ unless otherwise noted)

FIG.1 FORWARD CURRENT DERATING CURVE

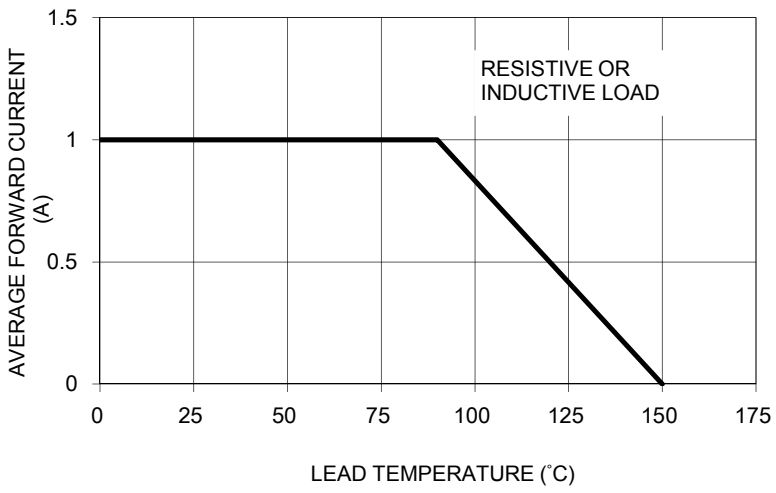


FIG. 2 TYPICAL REVERSE CHARACTERISTICS

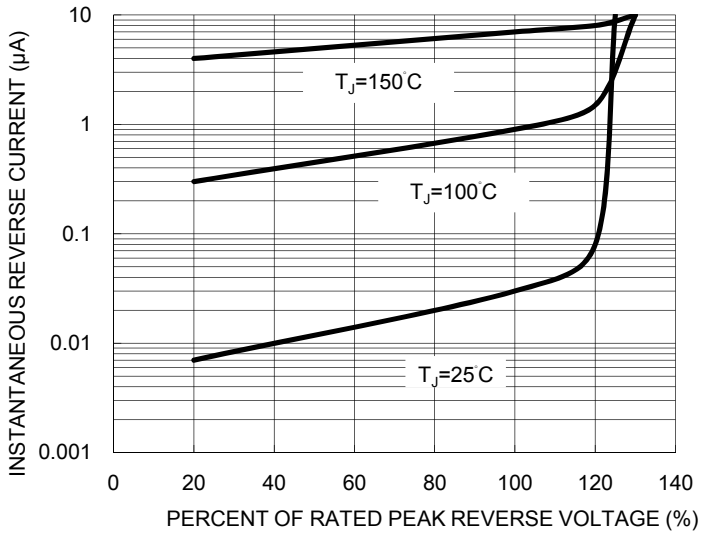


FIG. 3 MAXIMUM NON-REPETITIVE FORWARD SURGE CURRENT

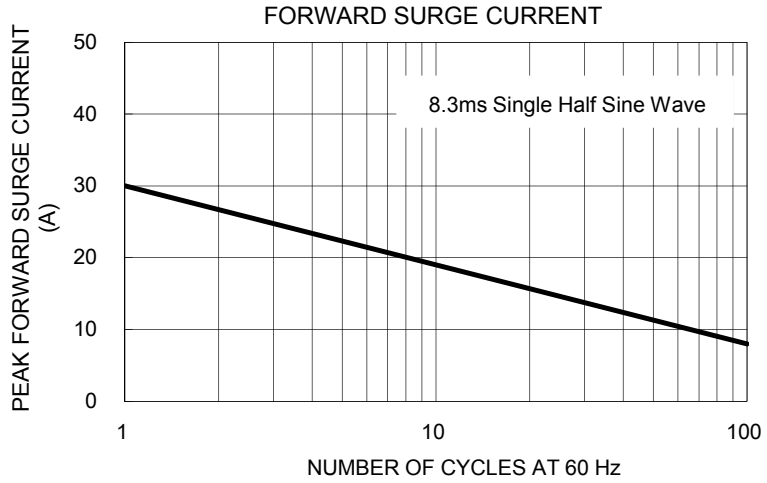


FIG. 4 TYPICAL FORWARD CHARACTERISTICS

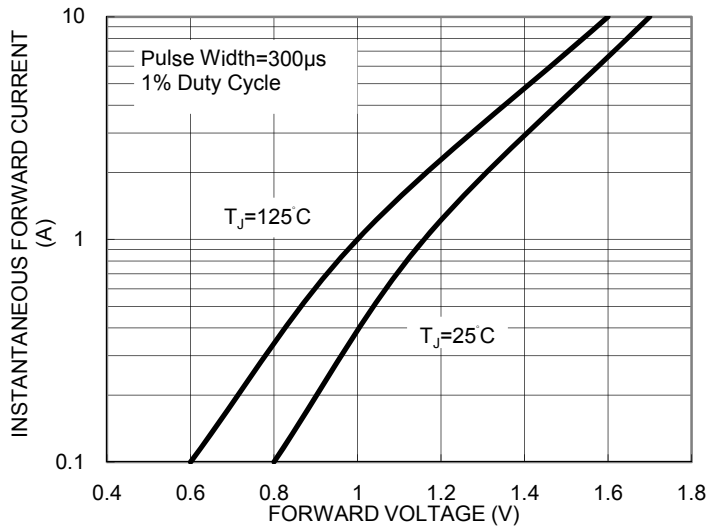


FIG. 5 TYPICAL JUNCTION CAPACITANCE

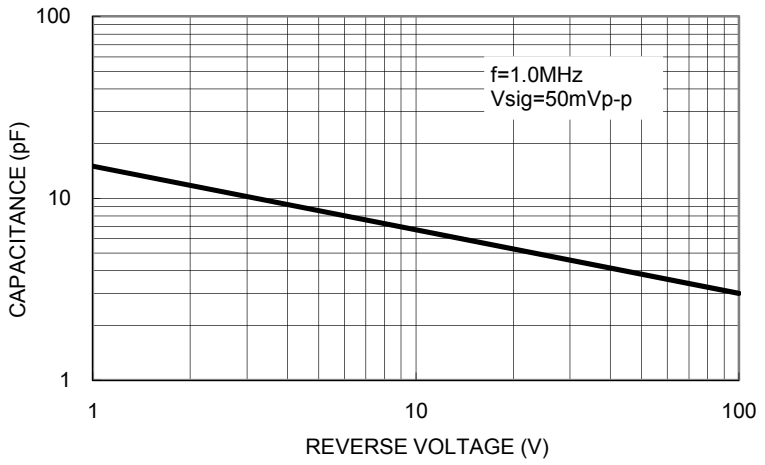


FIG.6- REVERSE RECOVERY TIME CHARACTERISTIC AND TEST CIRCUIT DIAGRAM